

August 20, 2003

AS
all required parameters and information that relate to the complete configuration of the compact flash memory card. In addition, the compact flash controller, at step 333, also designates one or more data blocks to be used for data block and data sector replacement.

IN THE CLAIMS

✓
Please amend the claims to read as shown below:

AP
Sub B1
1. (Currently Amended) A method of carrying out a data transfer to and from a flash memory array performed by a compact flash controller comprising the steps of:

inserting and powering up a compact flash memory device containing a plurality of compact flash memory arrays;

detecting presence of a plurality of compact flash memory arrays wherein the compact flash controller detects the number of compact flash memory arrays that comprise the compact flash memory device;

initializing controller, a plurality of flash memory ~~modules~~ arrays as well as other internal components;

partitioning each of the flash memory arrays in accordance to the parameters of ~~the~~ a configuration information table stored in a read-only memory of the compact flash controller;

determining which interface specification is to be used ~~for~~ to transfer data, address information and control signals to and from ~~the~~ a host device;

detecting a command sequence to be processed;

August 20, 2003

AP
Sub B1
translating the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair; and

executing the specified data transfer.

2. (Currently Amended) The method as recited in claim 1, wherein if the state of the received signal is high then a PCMCIA/ATA interface is selected to receive and transfer data, address information between flash memory and a host device.

3. (Currently Amended) The method as recited in claim 1, wherein if the state of received signal is low then a true IDE interface is selected to receive as well as transfer of data, ~~address information~~ between flash memory and a host device.

4. (Currently Amended) The method as recited in claim 1, wherein the set of data transfer operative elements that has been translated from the specified command sequence directs the compact flash controller to ~~writes~~ write data and address content received from the host device to at least one sector of a flash memory array pair.

5. (Currently Amended) The method as recited in claim 1, wherein the set of data transfer operative elements that has been translated from the specified command sequence directs the compact flash controller to ~~reads~~ read data and address content from at least one sector of a flash memory array pair.

6. (Original) The method as recited in claim 1, wherein the compact flash controller continues to perform each of the data transfer operative elements until a data transfer is complete.

7. (Currently Amended) The method as recited in claim 1, wherein the compact flash controller stands by waiting for a predetermined time period for the next data transfer operation.

August 20, 2003

AP 8. (Currently Amended) The method as recited in claim 7, wherein after if the a predetermined time period elapses, the compact flash controller suspends any operative activity and waits until a request to execute a new command sequence is detected.

Sub B1 9. (Currently Amended) A system for controlling the transfer of data between flash memory and a host device comprising:

circuitry of the compact flash controller configured to insert and power up a compact flash memory device containing a plurality of compact flash memory arrays;

circuitry of the compact flash controller configured to detect presence of a plurality of compact flash memory arrays wherein the compact flash controller detects the number of compact flash memory arrays that comprise the compact flash memory device;

circuitry of the compact flash controller configured to initialize controller, a plurality of flash memory modules as well as other internal components;

circuitry of the compact flash controller configured to partition each of the flash memory arrays in accordance to the parameters of the a configuration information table stored in a read-only memory of the compact flash controller;

circuitry of the compact flash controller configured to determine which interface specification is to be used for to transfer data, address information and control signals to and from the host device;

circuitry of the compact flash controller configured to detect a command sequence to be processed;

August 20, 2003

Ab
circuitry of the compact flash controller configured to translate the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair; and

Sub B1
circuitry of the compact flash controller configured to execute the specified data transfer.

10. (Original) The system as recited in claim 9, wherein the circuitry of the compact flash controller initiates PCMCIA/ATA interface is selected to receive as well as transfer of data, address information between flash memory and a host device, if the state of the received signal is high.

11. (Currently Amended) The ~~apparatus~~ system as recited in claim 9, wherein the circuitry of the compact flash controller initiates IDE interface is selected to receive as well as transfer of data, address information between flash memory and a host device, if the state of the received signal is low.

12. (Currently Amended) The ~~apparatus~~ system as recited in claim 9, wherein the circuitry of the compact flash controller initiates a write to at least one data sector of a flash memory array of data and address content received from the host device, if the the set of data transfer operative elements translated from the command sequence command specifies such an operation.

13. (Currently Amended) The ~~apparatus~~ system as recited in claim 9, wherein the circuitry of the compact flash controller initiates a read from at least one data sector of a flash memory array of the stored data and address content, if the set of data transfer operative elements translated from the command sequence specifies such an operation.

August 20, 2003

Ap 14. (Currently Amended) The ~~apparatus~~ system as recited in claim 9, wherein the circuitry of the compact flash controller continues to perform each of the data transfer operative elements until the data transfer is complete.

Sub B1 15. (Currently Amended) The ~~apparatus~~ system as recited in claim 9, wherein the circuitry of the compact flash controller stands by waiting a predetermined time period for the next data transfer operation.

16. (Currently Amended) The ~~apparatus~~ system as recited in claim 15, wherein the circuitry of the compact flash controller suspends any operative activity and waits until a request to execute a new command sequence to be detected, if the a predetermined time period elapses.

17. (Currently Amended) A computer program product that includes a computer useable medium having computer readable code embodied therein controlling the transfer of data between flash memory and a host device, the computer program product comprising:

a computer readable program code devices of the compact flash controller configured to insert and power up a compact flash memory device containing a plurality of compact flash memory arrays;

a computer readable program code devices of the compact flash controller configured to detect presence of a plurality of compact flash memory arrays wherein the compact flash controller detects the number of compact flash memory arrays that comprise the compact flash memory device;

a computer readable program code devices of the compact flash controller configured to initialize controller, a plurality of flash memory ~~modules~~ arrays as well as other internal components;

August 20, 2003

Δ
a computer readable program code devices of the compact flash controller configured to partition each of the flash memory arrays in accordance to the parameters of the a configuration information table stored in a read-only memory of the compact flash controller;

Sub B1
a computer readable program code devices of the compact flash controller configured to determine which interface specification is to be used for to transfer data, address information and control signals to and from the host device;

a computer readable program code devices of the compact flash controller configured to detect a command sequence to be processed;

a computer readable program code devices of the compact flash controller configured to translate the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair; and

a computer readable program code devices of the compact flash controller configured to execute the specified data transfer.

18. (Currently Amended) The computer program product as recited in claim 17, wherein if the state of the received signal is high then the computer readable program code devices of the compact flash controller initiates a PCMCIA/ATA interface is selected to receive as well as transfer of data, ~~address information~~ between flash memory and a host device.

19. (Currently Amended) The computer program product as recited in claim 17, wherein if the state of the received signal is low then the computer readable program code devices of the compact flash controller initiates a true IDE interface is selected to receive as well as transfer of data, ~~address information~~ between flash memory and a host device.

August 20, 2003

20. (Currently Amended) The computer program product as recited in claim 17, wherein the computer readable program code devices of the compact flash controller writes content received from the host device to at least one sector of a compact flash memory array pair, ~~data and address content received from the host device.~~

21. (Currently Amended) The computer program product as recited in claim 17, the computer readable program code devices of the compact flash controller reads data and address content from at least one sector of a compact flash memory array pair ~~data and address content~~ that is transferred back to the host device.

22. (Original) The apparatus as recited in claim 9, the computer readable program code devices of the compact flash controller continues to perform each of the data transfer operative elements until the data transfer is complete.

23. (Currently Amended) The computer program product as recited in claim 17, the computer readable program code devices of the compact flash controller stands by waiting for a predetermined time period for the next data transfer operation.

24. (Original) The computer program product as recited in claim 23, the computer readable program code devices of the compact flash controller suspends any operative activity and waits until a request to execute a new command sequence to be detected, if the a predetermined time period elapses.

***** R*E*M*A*R*K*S *****

Applicant herewith submits this Amendment in a bona fide attempt to advance the prosecution of this case and to answer each and every ground of rejection as set forth by the Examiner. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments to the specification and claims, and the remarks set forth below.